

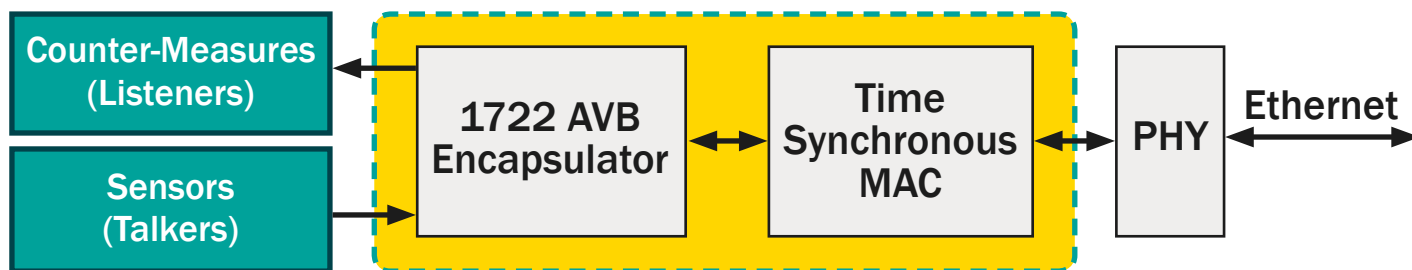
MAF Endpoint FPGA IP

AVB Capable MAC forward looking to TSN

Today's battles are being fought *smarter*, not just harder, and **Modular Active Protection Systems (MAPS)** are providing the latest weapon against oncoming threats, by connecting sensors that detect oncoming RPGs to the leading-edge defense systems that can disable them mere inches from a transport vehicle's exterior.

The DornerWorks **MAPS Framework (MAF) Endpoint FPGA IP** is custom designed to meet the demands for MAPS. This standards based MAC features an integrated and highly accurate gPTP module with 8ns accuracy and credit-based and strict-priority scheduling. The 1722 AVB Encapsulator simplifies integration into existing systems. Simply stream sensor data in to the IP and it's on the wire.

This IP was developed for the most demanding MAF systems, so you can be sure *it's the right solution for yours*.



Key Capabilities

- 1Gbs full-duplex MAC (IEEE 802.3)
- IEEE 1722 Data encapsulation for Synchronous and Asynchronous channels
- Automatic gPTP (IEEE 802.1AS-REV; slave-only)
 - +/- 8 ns accuracy
 - Rapid time synchronization convergence
- High precision packet prioritization and scheduling
- RGMII and SGMII interfaces with COTS PHY with MDIO
- User-configurable time-based triggers
- One PPS output signal with configurable hold-up time
- Supports 8 QoS priority levels / traffic classes, each with configurable strict-priority and credit-based scheduler (IEEE 802.1Q-2014)
 - IEEE 1722 Data encapsulators connect to 3 QoS priority levels, leaving 5 open for other traffic classes
- Streaming IP with no packet buffering minimizes latency and maximizes determinism
- Xilinx AMBA/AXI4 Lite and Stream interface



Start developing
your project
with us!



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Engineering Expertise

DornerWorks engineers are experienced at implementing time-synchronization and deterministic communication of devices across a COTS network, drawing on a mastery of hardware, software, and custom logic development.

The **MAF Endpoint FPGA IP** with built-in high-accuracy time-synchronization and features to support deterministic communication, and help you complete your next project successfully, *without frustration*.

Ideal for your system

- High-accuracy automated time-synchronization of networked devices, “behind the scenes”
- Low latency and highly deterministic transmission
- Traffic prioritization, bandwidth reservation and enforcement (ensures most important traffic will not be affected by least important traffic)
- Ideal for both new devices and retrofitting legacy devices



Developed for MAF

The FPGA logic in DornerWorks MAF Endpoint IP solution was developed for Xilinx FPGAs. As part of the MAC IP, it enables support for multiple types of heterogeneous traffic over a common network to reduce infrastructure costs.

As one of only three **Xilinx Alliance Program Premier Partners** that offer design services in North America, DornerWorks has guided many clients to successful product launches with custom hardware and software development.



Get started today!

Our simple 3-step plan will determine a technology development course of action that best fits your needs.



Start

Develop



Deliver

